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SEMICONDUCTOR DEVICE MANUFACTURING METHOD

Inventor: Akihiro Fuse
Ricoh Applied Electronics Research Laboratory, Ltd.
5-10 Yogataue, Aza, Kumanodo, Takadachi, Natori-shi, Miyagi-ken

Applicant: 000006747
Ricoh Co., Ltd.
1-3-6 Nakamagome, Ota-ku, Tokyo

Agent: Shigeo Noguchi, patent attorney

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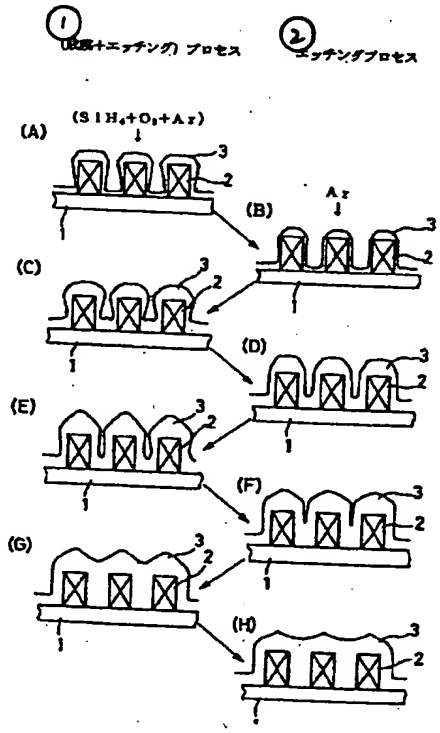
Abstract

Objective

The objective of the present invention is to form an insulating film with good reliability and excellent step coverage and controllability and with reduced damage to the semiconductor device by means of the bias ECR plasma CVD method.

Constitution

First, film-forming supply gas and argon gas are supplied, and bias ECR plasma CVD operation is performed for a prescribed period of time to form silicon oxide film (3) with a certain amount of overhang on metal wiring (2) as shown in (A). Then, the supply of the film-forming supply gas is stopped, and the sputter-etching operation is performed for a prescribed time, with the overhang of silicon oxide film (3) selectively etched to form the shape shown in (B). Then, further bias ECR plasma CVD operation and sputter-etching are carried out repeatedly, so that finally, as shown in (H), insulating film (3) that buries the portion between metal wiring portions (2), (2) free of voids and planarized to have excellent step coverage is formed.



Key: 1 (Film-formation + etching) process
2 Etching process

Claims

1. A semiconductor device manufacturing method characterized by an operation for forming an insulating film on a substrate using ECR plasma CVD wherein an RF bias is applied to the substrate, and the following two steps are carried out repeatedly during said operation for forming the insulating film:

a first step in as while a low-power RF bias is applied to the substrate, a film-forming supply gas and a gas containing an element that forms cations during ionization are fed in at the same time, so that film formation and sputter-etching by the cations are carried out at the same time; and

a second step in which, as a low-power RF bias is applied and the film-forming supply gas is not supplied, only the gas containing an element that forms cations in during ionization is supplied to perform only sputter-etching.

2. The semiconductor device manufacturing method described in Claim 1 characterized by the fact that the RF bias power applied to the substrate is in the range of 50-500 W.

3. The semiconductor device manufacturing method described in Claim 1 or 2 characterized by the fact that if the film-formation rate in said first step is A (Å/min), the film forming time for each cycle of said first step is t_1 (min), the etching rate of said second step is B (Å/min), and the etching time for each cycle of said second step is t_2 (min), then the following relationship is established by selecting the conditions appropriately:

$$0.4 \leqq A \cdot t_1 / B \cdot t_2 \leqq 2.0$$

Detailed explanation of the invention

[0001]

Industrial application field

The present invention pertains to a semiconductor device manufacturing method, in which a process for forming an insulating film, such as interlayer insulating film or passivation film, etc., is included in the manufacturing process of a semiconductor integrated circuit. In particular, the present invention pertains to a semiconductor device manufacturing method characterized by the fact that during the manufacturing process of semiconductor integrated circuit, said interlayer insulating film, passivation film, or other insulating film is formed by means of bias ECR plasma CVD.

[0002]

Prior art

At present, in the manufacturing process of LSI (large-scale integrated circuit) and other semiconductor devices, extensive studies are being made on using ECR (Electron Cyclotron Resonance) plasma CVD as a means of forming interlayer insulating films or passivation films. The ECR plasma CVD method has many advantages. For example, it allows film formation at a low temperature, and the magnitude of the energy of the radicals and ions used in this method is constant. Also, compared with conventional RF plasma CVD, there is less damage to the substrate under the plasma. In addition, it allows film formation in the high-vacuum region.

[0003]

Also, a bias ECR plasma CVD has been proposed. In this method, as an RF bias is applied to the substrate, argon gas or another gas is added to perform sputter-etching when the film is formed. As a result, step coverage is improved. In the bias ECR plasma CVD method, an RF bias is applied to the substrate, and the cations formed by ionization in ECR plasma are attracted by the self-bias effect due to the ion sheath generated near the substrate, and the effect of sputter-etching with the cations is exploited. Because the sputter-etching appears significantly in the slope portion of the surface of the substrate, the overhang of the insulating film is selectively etched, so that the regions between the metal wiring can be embedded without voids. Consequently, this method has attracted much attention.

[0004]

Usually, bias ECR plasma CVD pertains to competing reactions since film formation and etching are carried out at the same time. The sputter-etching rate is proportional to the magnitude of the RF power applied to the substrate. A characteristic feature of ECR plasma CVD is that it can realize a sputter-etching rate that can counter the high film-formation rate. Consequently, usually, in the bias ECR plasma CVD, the RF power applied to the substrate is at least 600 W, usually about 1 kW.

[0005]

However, although such a high RF bias improves the step coverage, such an application of high RF power leads to the following problems. First, due to the sputtering of argon ions and other cations, the metal wiring itself is etched, so that the service life of the metal wiring is reduced. Also, the surface of the insulating film becomes charged, so that the localized discharge between the surface of the substrate and the plasma takes place, leading to the generation of foreign particles and significant degradation of the surface. These are significant problems

confronting the formation of laminated wiring. Also, usually, in the bias ECR plasma CVD method, because film formation and sputter-etching are carried out at the same time and are competing reactions, it is difficult to set the operating conditions appropriately.

[0006]

In order to solve the aforementioned problems, several methods have been proposed. Japanese Kokai Patent Application No. Hei 3[1991]-280539 proposed a method in which during the initial stage of insulating film formation, the RF bias is not applied, or only a low-power RF bias is applied, so that no damage to the metal wiring takes place, followed by application of a high-power RF bias to form the insulating film. However, although this method can reliably avoid damage to the metal wiring, during the insulating film formation step, when an even higher RF bias, e.g., 600 W, is applied, the surface of the insulating film inevitably becomes charged, and localized discharge leads to generation of foreign particles and breakdown of the insulation.

[0007]

Another method, disclosed in Japanese Kokai Patent Application No. Hei 3[1991]-52232 proposes a method in which, first, no RF bias is applied to the substrate, and argon or another sputtering gas is not supplied so that only film formation is carried out. Then, an RF bias is applied and argon or another cation containing gas is used to perform sputter-etching, which processes are carried out repeatedly. However, because the film formation step and the sputter-etching step are performed separately and repeatedly in this method, the characteristic feature of the bias ECR plasma CVD, that is, improvement of step covering by means of simultaneous film-formation and sputter-etching, cannot be exploited at all. Consequently, the following problems arise. Usually, it is well known that in the case of ECR plasma CVD, when the film is formed without applying an RF bias to the substrate, the insulating film formed on the metal wiring will be deposited with an overhang. This overhang is a major cause of voids in regions between the metal wiring parts. In the case of ECR plasma CVD, usually, the film-formation rate is high. It may be in the range of several thousand Å/min to several μm/min. Consequently, with progress in developing finer semiconductor device elements and metal wiring, the problem of the generation of voids due to overhang becomes a dominant factor in a very short time after the start of the insulating film. Even when sputter-etching is later carried out, the voids still cannot be eliminated. In order to solve this problem, if, e.g., the film-formation rate is 1 μm/min and the line-and-space (L/S) of the design rule is 0.5 μm/0.5 μm, then the time after the start of the film-formation must be controlled to about 10-20 sec. However, since the plasma state is unstable and regeneration is poor, the process becomes more unstable, which is undesirable.

[0008]

Problems to be solved by the invention

The objective of the present invention is to solve the aforementioned problems of the conventional methods by providing a method for manufacturing semiconductor device characterized by the fact that while the characteristic features of the bias ECR plasma CVD method are maintained, an insulating film with high reliability is formed with good controllability, excellent step coverage, and suppression of damage to the semiconductor device.

[0009]

Means to solve the problems

The present invention pertains to a semiconductor device manufacturing method characterized by the fact that in the semiconductor device manufacturing method, which includes an operation for forming an insulating film on a substrate using ECR plasma CVD that can apply an RF bias to the substrate, the following two steps are carried out repeatedly during said operation for forming the insulating film: a first step in which while a low-power RF bias is applied to the substrate, a film-forming supply gas and a gas containing an element that forms cations during ionization are supplied at the same time, so that the film formation and sputter-etching by the cations are carried out at the same time; and a second step in which while a low-power RF bias is applied, while the film-formation supply gas is not introduced, only the gas containing the element that forms cations during ionization is supplied to perform only sputter-etching.

[0010]

In a preferable embodiment, the power of the RF bias applied to the substrate is in the range of 50-500 W. As far as the preferred conditions for the present invention are concerned, if the film-formation rate during said first step is A (Å/min), the film-formation time for each cycle of said first step is t_1 (min), the etching rate of said second step is B (Å/min), and the etching time for each cycle of said second step is t_2 (min), the following relationship is established by selecting the conditions appropriately:

$$0.4 \leqq A \cdot t_1 / B \cdot t_2 \leqq 2.0$$

[0011]

The ECR plasma CVD apparatus used in the present invention is an ECR plasma CVD apparatus that allows application of an RF bias to the substrate. Although the conventionally prepared RF power source has an output that can go to 1 kW or even higher, according to the

present invention, a low-power RF bias is used. Consequently, an RF power source of up to 500 W is sufficient.

[0012]

According to the present invention, the gas used for sputter-etching may be any gas that contains an element which can be ionized to form cations. Usually, Ar (argon) gas is selected because it has a high sputtering efficiency and can be handled easily. Because He (helium) may also be ionized to provide He ions, it may be used by itself or mixed with Ar gas. As far as the supply gas for forming the insulating film is concerned, when the film to be formed is silicon oxide film, silane (SiH_4) and oxygen are preferred. On the other hand, when the film to be formed is silicon nitride film, silane and nitrogen are preferred.

[0013]

Application examples

Figure 1 illustrates the processing steps for forming a silicon oxide film according to the present invention. In this example, silane and oxygen are used as film-formation gas, and argon is used as the gas for sputtering. In this figure, (A), (C), (E) and (G) illustrate the shape after the so-called bias ECR plasma CVD step in which both the film forming supply gas and sputtering gas are introduced. On the other hand, (B), (D), (F) and (H) illustrate the shape after the sputter-etching step in which only the sputtering gas is fed in. In both steps, the output of the RF bias applied to the substrate is 250 W.

[0014]

First, when the bias ECR plasma CVD step is carried out for a prescribed time, as shown in (A), silicon oxide film (3) with a certain amount of overhang is formed on metal wiring (2) on substrate (1). In the conventional bias ECR plasma CVD, in order to avoid the generation of this overhang, a high-power RF bias is applied. However, in the present invention, since there is a subsequent sputter-etching step, a certain amount of overhang can be tolerated.

[0015]

The introduction of the film-formation gas is then stopped, and the sputter-etching step is initiated. After the sputter-etching step is performed for a prescribed length of time, the overhang is selectively sputter-etched, resulting in the shape shown in (B). After bias ECR plasma CVD step is carried out, the shape appears as shown in (C). Sputter-etching is then carried out, and the shape appears as shown in (D).

[0016]

In this way, since the bias ECR plasma CVD and sputter-etching processing steps are performed repeatedly in that order as shown in (H), insulating film (3) that buries up the portion between metal wiring parts (2), (2) without voids, and is flattened to produce excellent step coverage is formed. In this way, since bias ECR plasma CVD and sputter-etching steps are performed repeatedly, even with a low-power RF bias, an insulating film with excellent step coverage can still be formed with reduced damage to the semiconductor device.

[0017]

Application Example 1

On a 4-inch single crystal silicon wafer, a thin aluminum film with a thickness of about 9000 Å was formed using a conventional method. By means of photolithography and etching, a pattern with line-and-space (L/S) of 0.7 μm/0.7 μm was formed on the substrate. The conditions for bias ECR plasma CVD and sputter-etching were the following.

[0018]

Bias ECR plasma CVD step

Flow rate of SiH_4: 10 sccm

Flow rate of O_2: 15 sccm

Flow rate of Ar: 20 sccm

Sputter-etching step

Flow rate of Ar: 20 sccm

In both processing steps, the pressure was set to 1 mtorr, the substrate temperature was set to 150°C, the microwave power was 700 W, and the RF (13.56 MHz) power was 250 W.

[0019]

The conditions for the various processing steps were selected as follows. The unit time for each cycle of the bias ECR plasma CVD step was 3 min, the unit time for each cycle of the sputter-etching step was 5 min, and these steps were performed alternately, 8 cycles each. As a result, a silicon oxide film embedded between the metal wiring parts without voids and with a flat surface was obtained.

[0020]

Application Example 2

The operation was performed in the same way as in Application Example 1, except that the line-and-space (L/S) of the substrate was selected as 0.5 μm/0.5 μm, the unit time for each cycle of the bias ECR plasma CVD step was 2 min, the unit time for each cycle of the sputter-etching step was 6 min, and these steps were performed alternately, 8 cycles each. As a result, a silicon oxide film embedded between the metal wiring parts without voids and with a flat surface was obtained.

[0021]

In the first step, that is, the bias ECR plasma CVD step, the film-formation rate was A (Å/min), and the film-formation time for each cycle of operation, that is, the unit time of the first processing step, was t_1 (min). In the second step, that is, the sputter-etching step, the film-formation rate was B (Å/min), and the film-formation time for each cycle of operation, that is, the unit time for the second processing step was t_2 (min).

[0022]

Figure 2 is a diagram illustrating the film-formation rate of silicon oxide film formed using the bias ECR plasma CVD method while the RF bias power applied to the substrate was changed to different levels. When the RF bias power is 0, the film-formation rate is about 800 Å/min. On the other hand, film-formation rate A, when an RF bias power of about 250 W is applied, is about 600 Å/min, as can be read from the graph. From this result, one can see that when an RF bias of 250 W is applied, the obtained apparent etching rate B is 800-600 = 200 (Å/min)

Here, the repeating periods of the two steps are evaluated by means of the ratio of product $A \cdot t_1$ (where A represents the film-formation rate of the first step, and t_1 represents its unit time) to product $B \cdot t_2$ (where B represents the film-formation rate of the second step, and t_2 represents its unit time), $A \cdot t_1 / B \cdot t_2$.

[0023]

With Application Examples 1 and 2 included, conditions were further changed to perform measurements. The regions between metal wiring parts were examined to determine the presence of voids. The results are listed in Table I.

[0024]

Table 1

①条件	$A \cdot t_1 / B \cdot t_2$	L/S =0.7/0.7(μm)	L/S =0.5/0.5(μm)
(5, 3)×5	5.0	×	×
(4, 4)×6	3.0	×	×
(3, 5)×8	1.8	○	×
(2, 6)×8	1.0	○	○
(1, 7)×10	0.4	○	○

Key: 1 Condition

[0025]

In the conditions column, for example, (5, 3)x5 means that the unit time of the first step is 5 min, the unit time of the second step is 3 min, and the repetition cycle number is 5. The smaller the line-and-space (L/S), the more difficult it is to form a good insulating film. In the table, a O indicates that the interlayer film is well embedded between metal wiring portions without voids, and an X indicates that voids are present.

[0026]

Effect of the invention

According to the present invention, the bias ECR plasma CVD at low-power RF bias and the sputter-etching processing steps are carried out repeatedly. As a result, it is possible to suppress damage to the semiconductor device when an insulating film with a flat surface and excellent step coverage is formed to bury the regions between metal wiring parts without voids. Also, according to the present invention, the operation is composed of repeated ECR plasma CVD and sputter-etching steps. By controlling the length of time and number of cycles, it is possible to optimize the parameters to form various wiring dimensions. Consequently, the regeneration property is good, and controllability is also excellent.

Brief description of the figures

Figure 1 presents cross-sectional views illustrating the processing steps for forming a silicon oxide film in an application example of the present invention.

Figure 2 is a diagram illustrating the film-formation rate versus RF bias power in an application example of the present invention.

Explanation of symbols

1 Silicon substrate

2 Metal wiring

3 Silicon oxide film

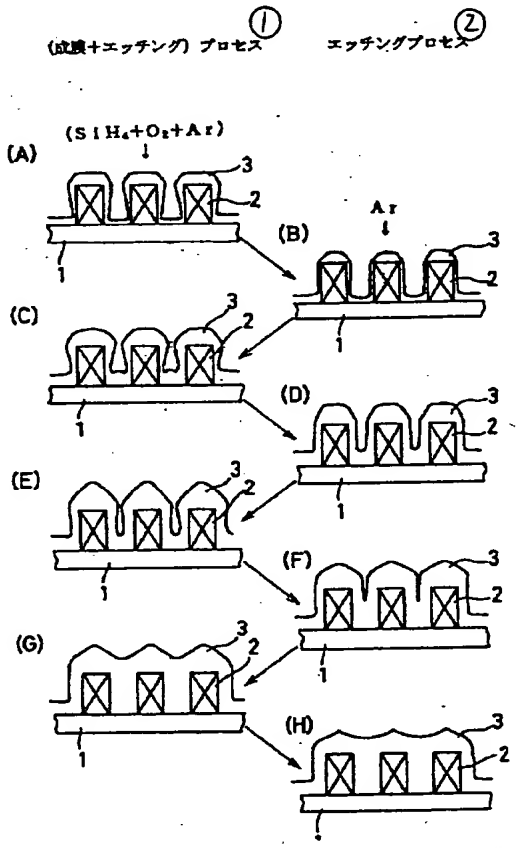


Figure 1

Key: 1 (Film-formation + etching) process

2 Etching process

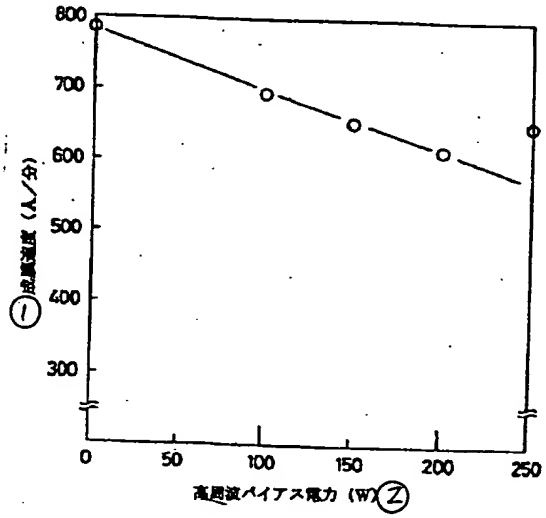


Figure 2

Key: 1 Film-formation rate (Å/min)
2 RF bias power (W)